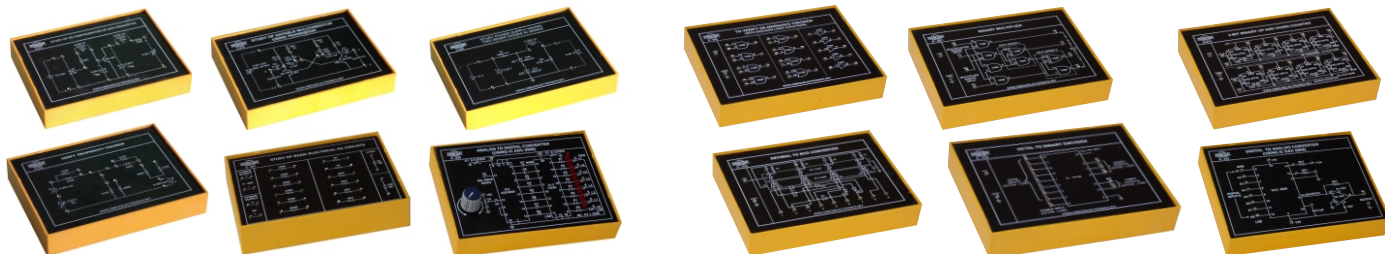


OPTIONAL MODULES :-

These are ready to use modules with wired components & circuit schematic drawn on top compatible to use out of below modules can be used with our Following Training Boards. Digital Lab (DL-1041), Analog Lab (AL-1042), Digital -Analog Lab (DAL-1043), Digital Trainer (DL-1044), Logic Lab (DL-1047), Digital Lab Station (DL-1049) Bread Board Circuit Lab (BBS-105), LTB-841, LTB-842, LTB-845.



ANALOG LAB MODULES

- A001. Study of Diode in DC circuits
- A002. Study of Light Emitting Diodes in DC Circuits
- A003. Study of Half wave rectifier
- A004. Study of Full wave rectifier
- A005. Study of Zener Diode as a voltage regulator
- A006. Study of transistor series voltage regulator
- A007. Study of transistor shunt voltage regulator
- A008. Study of Low pass filter
- A009. Study of High pass filter
- A010. Study of band pass filter
- A011. Study of CE configuration of NPN transistor
- A012. Study of CB configuration of NPN transistor
- A013. Study of CE amplifier
- A014. Study of Monostable multivibrator using transistor
- A015. Study of Bistable multivibrator using transistor
- A016. Study of Astable multivibrator using transistor
- A017. Study CB amplifier (PNP)
- A018. Study CC amplifier (PNP)
- A019. Study of FET amplifier.
- A020. Study power supply having two zener diodes in series
- A021. Study dual polarity voltage regulated power supply
- A022. Study the characteristics of photo transistor
- A023. To practically understand the operation of a 7-segment LED display
- A024. To Study CC configuration of NPN transistor
- A025. Study CE configuration of PNP transistor
- A026. Study CB configuration of PNP transistor
- A027. Study CC configuration of PNP transistor
- A028. Study full wave dual polarity supplies
- A029. Study of FET characteristic
- A030. Verify superposition theorem
- A031. Verify thevenin's theorem
- A032. Verify reciprocity theorem
- A033. Study of Phase shift audio oscillator (Solid State)
- A034. Verify kirchoff's law (V & I)
- A035. Verify ohm's law
- A036. Ideal resistance characteristics
- A037. Verification of series law of resistance
- A038. Verification of parallel law of resistance
- A039. Verify maximum power transfer theorem
- A040. Study of series and parallel resistance, capacitors and inductance circuits
- A041. Study of basic electrical DC circuits
- A042. Study of AC circuits
- A043. Study of series and parallel resonance and operational amplifier circuits
- A044. Study of power supply circuit, 555 timer and solid state switch
- A045. Study of difference Amplifier
- A046. Analog to digital converter (using IC ADC 0800)

DIGITAL LAB MODULES

- D001 Logic gates operation
- D002 To verify De-morgan's theorem with boolean logic equations
- D003 Binary to Gray code conversion
- D004 Gray code to Binary conversion
- D005 Binary to Excess-3 code conversion
- D006 Binary Adder and Subtractor
- D007 Binary Multiplier
- D008 EX-OR gate implementation
- D009 Application of EX-OR gate
- D010 Johnson Counter
- D011 To verify the dual nature of Logic Gates
- D012 Study of Flip-Flops RS, JK, D&T
- D013 Multiplexer and Demultiplexer
- D014 4 Bit Binary up and down counter
- D015 Study of 8 to 3 Line Encoder
- D016 Study of 3 to 8 Line Decoder
- D017 Study of Shift Register (SIPO)
- D018 CMOS-TTL Interfacing
- D019 Study of Crystal oscillator
- D020 Study of pulse stretcher circuit
- D021 4 Bit Ring Counter
- D022 Modulo 12 Counter By Direct Clearing
- D023 Decade counter
- D024 Shift Register SISO and PIPO
- D025 Decimal to BCD Converter
- D026 Astable Multivibrator using Digital IC
- D027 Bistable Multivibrator using Digital IC
- D028 Monostable Multivibrator using Digital IC
- D029 Octal to binary Encoder
- D030 4 Bit Magnitude Comparator
- D031 Interface of TTL-IC to CMOS-IC & CMOS IC to TTL-IC
- D032 Digital to analog converter (using IC DAC 0808)

Weight : 0.7 Kg. (Approx)
Dimension : W 176 x H 131 x D 37

We are committed to the continuous development of our products. and therefore reserve the right to amend specifications without prior notice.

OMEGA ELECTRONICS