**OMEGA TYPE LTB – 892** The Electronic Sequencer  is intended for elementary as well as advance training of digital electronics. The trainer cover regular digital circuits by solder less inter connections through use of 4 mm brass terminations and patch cords. logic level input / output indicators and DC regulated power supply are in built. The unit housed in finished  box .

**THE TRAINER COVER THE FOLLOWING  EXPERIMENT :**
**EXPERIMENT 1 :** STUDY OF BASIC GATES AND VERIFICATION OF THEIR TRUTH TABLES.

| | |
|---|---|
| 1.1 | NOT |
| 1.2 | OR |
| 1.3 | AND |
| 1.4 | NOR |
| 1.5 | NAND |

**EXPERIMENT 2 :** STUDY AND VERIFICATIONS OF THE LAW OF BOOLEAN ALGEBRA AND DE-MORGAN'S THEOREMS.

| | |
|---|---|
| 2.1.1 | AND |
| 2.1.2 | OR |
| 2.1.3 | COMPLEMENT OR NOT |

**THEOREMS**

| | |
|---|---|
| 2.2.1 | $(A = A + 0)$ |
| 2.2.2 | $(1 = A + 1)$ |
| 2.2.3 | $(A = A + A)$ |
| 2.2.4 | $(1 = A + A')$ |
| 2.2.5 | $(A.1 = A)$ |
| 2.2.6 | $(A.0 = 0)$ |
| 2.2.7 | $(A.A = A)$ |
| 2.2.8 | $(A.A' = 0)$ |
| 2.2.9 | (a & b) De Morgan's Theorem-I    LHS & RHS $(A+B)' = A'. B'$ |
| 2.2.10 | (a & b ) De Morgan's Theorem -II   LHS & RHS $(A.B)' = A' + B'$ |
| 2.2.11 | $A + AB = A$ |
| 2.2.12 | $A + A'B = A + B$ |
| 2.2.13 | $(AB + AB') = A$ |
| 2.2.14 | $(a \& b)(AB + A'C) = (A + C)(A' + B)$ |
| 2.2.15 | $AB + A'C + BC = AB + A'C$ |
| 2.2.16 | $A(A + B) = A$ |
| 2.2.17 | $(a \& b)A(A' + B) = AB$ |
| 2.2.18 | $(A + B)(A + B') + A$ |
| 2.2.19 | $(A + B)(A' + C) = AC + A'B$ |
| 2.2.20 | $(a \& b)(A + B)(A' + C)(B + C) = (A + B)(A' + C)$ |

**EXPERIMENT3:** CONSTRUCTION AND VERIFICATION OF VARIOUS TYPES OF FLIP-FLOPS USING GATES AND IC'S

| | |
|---|---|
| 3.1.1 | RS Flip - Flop using NAND Gates |
| 3.1.2 | RS Flip - Flop using NOR gates |
| 3.1.3 | Clocked R - S Flip - Flop |
| 3.2.1 | J - K Flip - Flop |
| 3.2.2 | J - K Flip - Flop with Clocks |
| 3.2.3 | Master - Slave J - K Flip - Flop |
| 3.3 | D Flip - Flop |

**EXPERIMENT 4 :** CONSTRUCTION AND VERIFICATION OF VARIOUS TYPES OF COMBINATIONAL CIRCUITS

| | |
|---|---|
| 4.1 | 2 to 1 Line Multiplexer ( Encoder) |
| 4.2 | 2 to 4 Line Demultiplexer (Decoder) |
| 4.3 | 2 Bit Comparator |
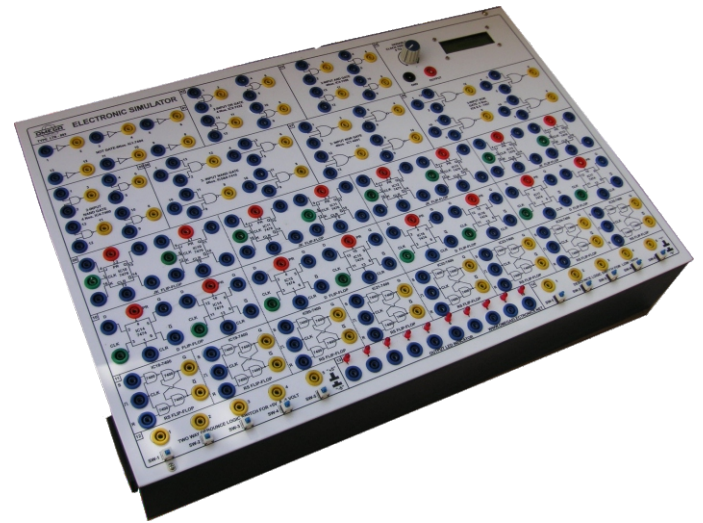


**EXPERIMENT 5 :** CONSTRUCTION AND VERIFICATION OF VARIOUS TYPES OF COUNTERS.

| | |
|---|---|
| 5.1 | 3 Bit Down counter |
| 5.2 | UP Counter |
| 5.2.1 | 3 Bit Synchronous Ripple UP Counter |
| 5.2.2 | 3 Bit Asynchronous Ripple UP Counter |
| 5.3 | Ring Counter |
| 5.4 | Decade Counter |

**FEATURE**

NOT Gate-Six Numbers Using 7404
Two Input OR Gate-Four Numbers Using-7432
Two Input AND Gate-Four Numbers Using-7408
Two Input NAND Gate-Four Numbers Using-7400
Three Input NAND Gate-Four Numbers Using-7410
Two Input NOR Gate-Four Numbers Using-4001
Three Input NOR Gate-Four Numbers Using-7427
D FLIP-FLOP Eight Numbers Using 7474
JK FLIP-FLOP Eight Numbers Using 7476
RS FLIP-FLOP Eight Numbers Using 7400

| | | |
|---|---|---|
| DC Power Supply | : | 5 V  / 500 mA (Int.) |
| Debounce Logic Switch | : | Five independent logic level inputs to select High / Low TTL levels, |
| Output LED Indicators | : | Ten independent logic level indicators for High / Low status indication of digital outputs. |
| Two Way Debounce | : | Five independent  logic level inputs to select levels For +5V &-5V Logic Switch |
| Variable Freq./Clock | : | 0 To 2 KHz With digital display |
| Power ON | : | Power ON switch with indicator for mains on indication and fuse for protection. |
| Patch Cords | : | Set of 20 assorted coloured multi-stand wires with 4mm stackable plug termination at both ends.(Stackable) |
| Power Requirement | : | 230V ± 10% single phase AC. |
| Instruction manual | : | One detailed instruction manual with well thought out experiments covering the above topics. |
| Weight | : | 5 Kg. (Approx). |

We are committed to the continuous development of our products, and therefore reserve the right to amend specifications without prior notice.